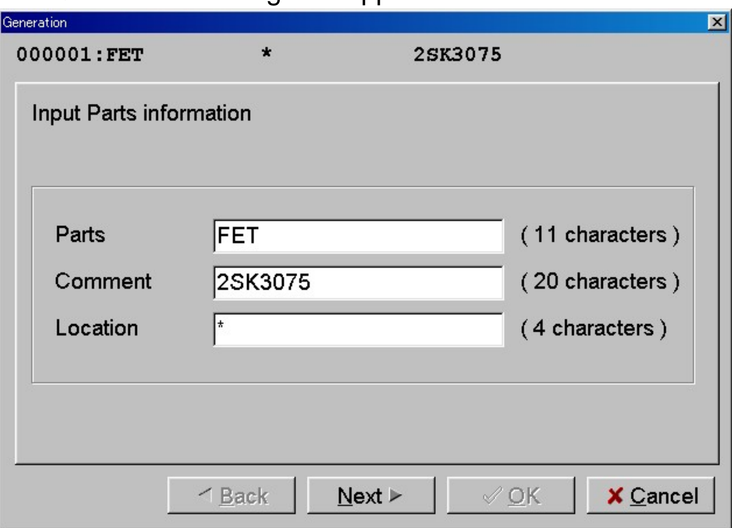
TAKAYA CORPORATION

# FET MEASUREMENT

**[TEST DATA PROGRAMMING ]**

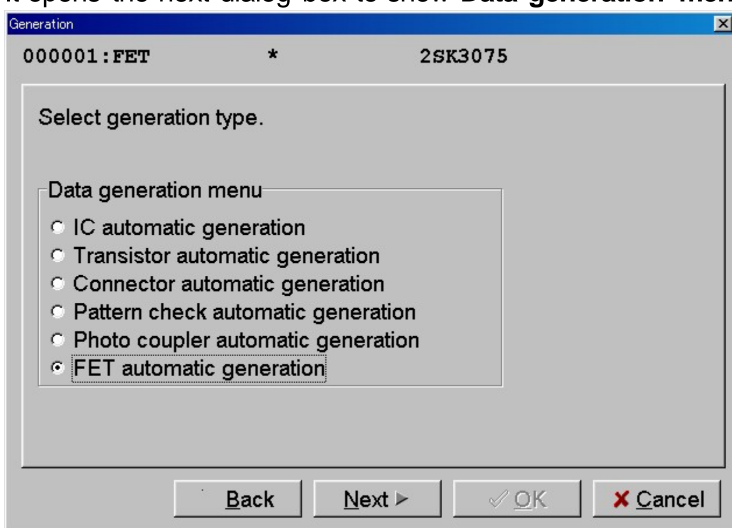
Open Generation dialog box (Tool > Auto Generation) on the Edit / List menu, so that you can make the test program of Field-Effect Transistor (FET) easily, as well as ICs, Transistors, etc.

1. Open the step list (Edit /List menu).
2. Move the cursor to the step where you want to generate FET measuring step.
3. Select: **Tool > Auto Generation**
4. The **Generation** dialog box appears.




Generation dialog box [Fig.1]

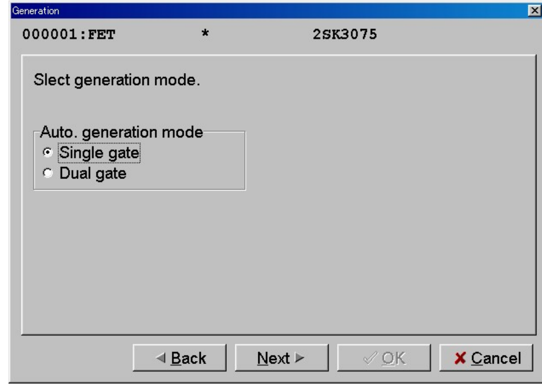
5. Fill Parts/Comment/Location edit box and then click the **Next** button.
6. It opens the next dialog box to show **Data generation menu.**




Data Generation Menu [Fig.2]

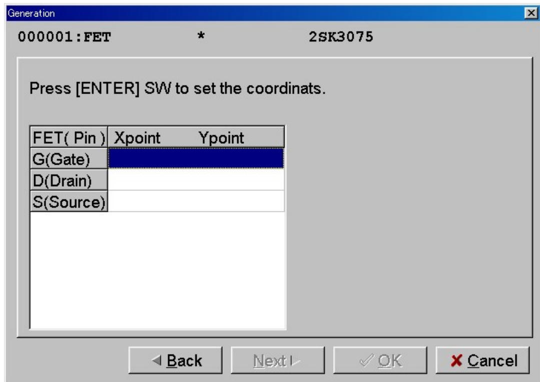
7. Fill **FET automatic generation** radio button and then click the **Next** button.

8. It opens the next dialog box to show **Auto. generation mode**.

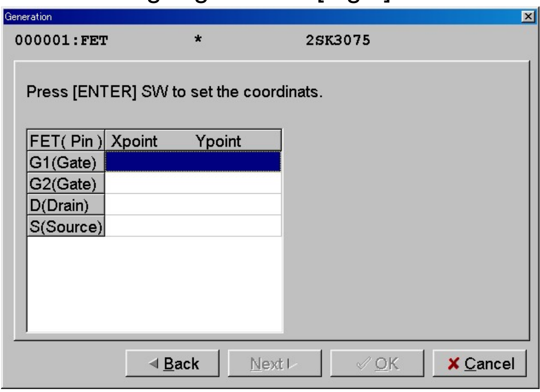



Auto. generation mode [Fig.3]

9. If [**Single gate**] was selected, it shows [Fig.4]. If [**Dual gate**] was selected, it shows [Fig.5]. Please input X,Y coordinate values for each device leads in the same manner as Transistors.

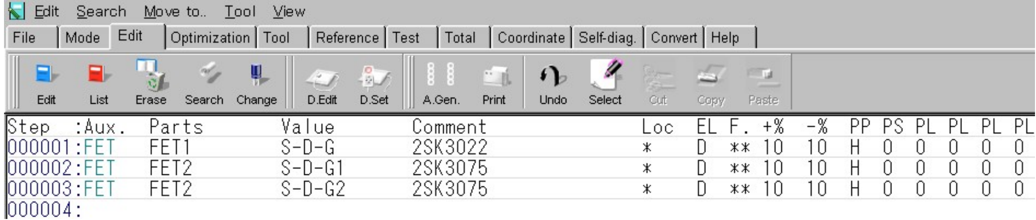



Single gate FET [Fig.4]




Dual gate FET [Fig.5]

10. The test data automatically generated is either 1 step only (=Single gate FET) or 2 steps (=Dual gate FET).




(Single gate FET > Step #1, Dual gate FET > Step #2 – 3 ) [Fig.6]

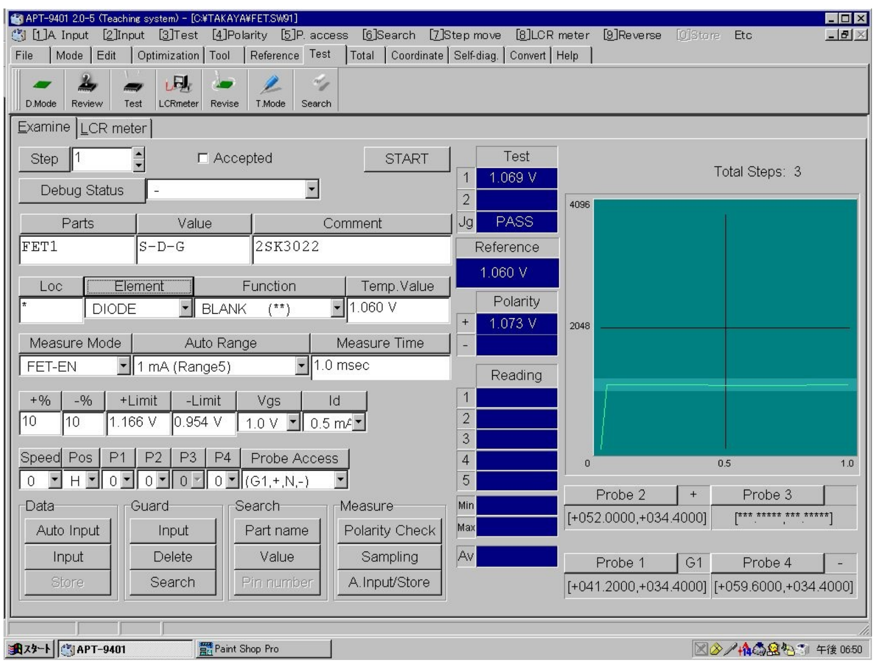
(NOTE1) In the test data automatically generated, the polarity of Gate(G) is substituted by either [G1] or [G2], Drain(D) is substituted by [+], and the Source(S) is substituted by [-].
In case of Single gate FET, however, it uses only [G1].
Also, the polarity of Drain(D) and Source(S) is automatically adopted when the reference value is input, according to the FET type which is either N-channel or P-channel.

(NOTE2) Name column of each FET step data is substituted by “S-D-G” (=Single gate FET), or both “S-D-G1” and “S-D-G2” (=Dual gate FET).

(NOTE3) “FET” is displayed in the “Aux” field.

**[EVALUATION MENU]**

The evaluation menu (Test > Review Step Data) for FET test steps will be just like [Fig.7].
They indicate Vgs (limit voltage between G-S) and Id (Constant current between D-S) in the measuring wave form window.

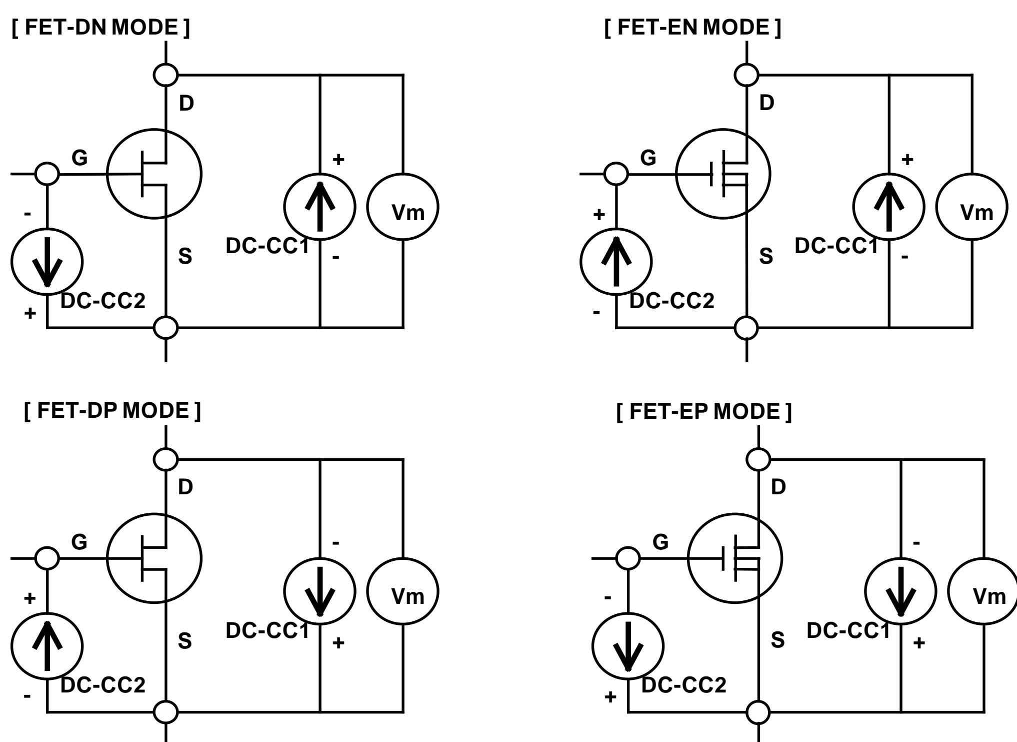



[Fig.7]

## ■ MEASURING MODE

To measure the Depletion mode FETs, the measuring mode “**FET-DN**” is used for N-channel and “**FET-DP**” is for P-channel. As for Enhancement mode FETs, the measuring mode “**FET-EN**” is used for N-channel and “**FET-EP**” is for P-channel. The composite type (Depletion mode + Enhancement mode) uses either “FET-D*” or “FET-E*” automatically .

Usually, the most adequate measuring mode is automatically adopted when the reference value is input. But you can change it between “FET-EN”,”FET-EP”,”FET-DN” and ”FET-DP” manually according to your preference.




**n MEASURING RANGE**

The measuring range DC-CC2 (Ig) can be substituted by any of 50uA, 100uA, 200uA, 500uA, 1mA, 2mA, 5mA, 10mA or 20mA automatically or manually. (=Constant current signal) Also, as the limit voltage, any of 0V, 0.5V, 1.0V, 1.5V, 2.0V, 2.5V, 3.0V or 5.0V can be selected automatically or manually. (However, 3.0V and 5.0V can be selected by manual only)
To appoint the limit voltage manually, assign it in Value column of the test data directly. (Ex. “0.5V”, “2.0V”, etc.)

The measuring range DC-CC1 (Id) can be substituted by either 500uA or 5mA automatically or manually. (=Constant current signal) The limit voltage is fixed to 1.0V.

**n REFERENCE VALUE**

The reference value is substituted by the “difference” of two voltage which were measured when the DC-CC2 measurin g signal was applied and not applied to the Gate.

**n REFERENCE INPUT, MEASUREMENT**

For the Single gate FETs, the DC-CC2 measuring signal is applied on between G-S, then G is connected to D to gain the same electric potential. Under this condition, the difference of two voltage of between G-S is measured, which were gain when the DC-CC2 measuring signal was applied, another is when it not applied.

For the Dual gate FETs, at first the DC-CC2 measuring signal is applied on between $G_1$-S, then $G_2$ is connected to D to gain the same electric potential. Under this condition, the difference of two voltage of between $G_1$-S is measured, which were gain when the DC-CC2 measuring signal was applied, another is when it not applied.

As the 2nd step, the DC-CC2 measuring signal is applied on between $G_2$-S, then $G_1$ is connected to D to gain the same electric potential. Under this condition, the difference of two voltage of between $G_2$-S is measured, which were gain when the DC-CC2 measuring signal was applied, another is when it not applied.

**n LIMITATIONS**

• When the resistance between "G-D" "G-S" and "S-D" was less 40ohm, it shows 'The guard point is not effective !' as the error message. (KEY0 'Save' is possible, but sometimes it cannot detect any failure.)

‚ For the FET measurement step, "Automatically Create Reference Value" (Reference > Reference Value Generation) cannot generate any reference value.

ƒ At the evaluation menu (Test > Review Step Data), even if KEY4(Polarity) was pressed, the measured value of minus (-) side does not appear.

„ At the evaluation menu (Test > Review Step Data), if the L-limit was less than 0.050V when the reference value was input, it shows "Range under !" as the error message. (KEY0 'Save' is impossible)

… If the difference of two voltage was less than 0.2V when the DC-CC2 measuring voltage was turned on/off, it shows "Un-measure !" as the error message. (KEY0 'Save' is possible, but sometimes it cannot detect any failure.)

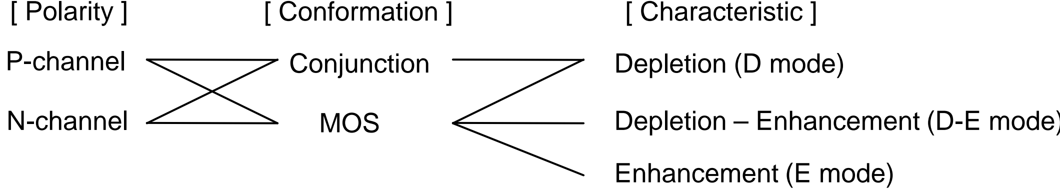
**[ SUPPLEMENTARY ]**

In general, the FETs are divided into two groups ; 'N-channel' and 'P-channel', and also classified by either 'Junction type' or ' MOS type' according to the difference of the internal conformation.

And, there are two remarkable types ; one is Single gate type and another is Dual gate type.

Also, there are classified by Depletion type (D mode), Depletion + Enhancement type (D+E mode) and Enhancement type (E mode), according to FET function mode.

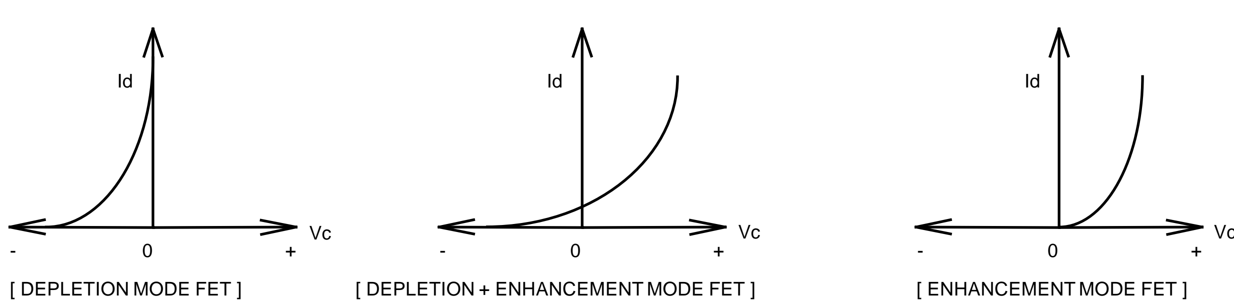
**n FET CLASSIFICATION**



## ■ FET SYMBOLS

| | JUNCTION TYPE | | MOS TYPE | |
|---|---|---|---|---|
| | SINGLE GATE TYPE | DUAL GATE TYPE | SINGLE GATE TYPE | DUAL GATE TYPE |
| N - CHANNEL | D G S / D G S | D G1 G2 S | D G S | D G1 G2 S / D G1 U (G2) S |
| P - CHANNEL | D G S / D G S | D G1 G2 S | D G S | D G1 G2 S / D G1 U (G2) S |

## ■ FET CHARACTERISTIC



[ DEPLETION MODE FET ] [ DEPLETION + ENHANCEMENT MODE FET ] [ ENHANCEMENT MODE FET ]

(REMARKS)

As mentioned, there are generally three different types of FET modes; “Depletion mode”, “Depletion + Enhancement mode” and “Enhancement mode”.

In case of Depletion mode FET, max. Current can flow between S-D when there is no electric potential between G-S. On the other hand, in Enhancement mode FET, no current can flow between S-D when there is no electric potential between G-S. Depletion + Enhancement mode FET has the intermediate characteristic of them.